

## 240pin Unbuffered DDR2 SDRAM MODULE

Based on 128Mx8 DDR2 SDRAM G-die

### Features

Performance:

		PC2-5300	PC2-6400	PC2-8500	
Speed Sort		-3C	-AC	-BD	Unit
DIMM $\overline{\text{CAS}}$ Latency		5	5	6	
f CK	Clock Frequency	333	400	533	MHz
t CK	Clock Cycle	3	2.5	1.875	ns
f DQ	DQ Burst Frequency	667	800	1066	Mbps

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 128Mx64 and 256Mx64 DDR2 Unbuffered DIMM based on Elixir 128Mx8 DDR2 SDRAM G-die component
- Double Data Rate architecture; two data transfer per clock cycle
- Differential bi-directional data strobe (DQS &  $\overline{\text{DQS}}$ )
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK &  $\overline{\text{CK}}$ )
- Intended for 333MHz/400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{\text{DD}} = V_{\text{DDQ}} = 1.8\text{V} \pm 0.1\text{V}$
- 7.8  $\mu\text{s}$  Max. Average Periodic Refresh Interval
- Programmable Operation:
  - Device  $\overline{\text{CAS}}$  Latency: 3, 4, 5, 6
  - Burst Length: 4, 8
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/rank) – 1GB
- 14/10/2 Addressing (row/column/rank) – 2GB
- Serial Presence Detect
- On Die Termination (ODT)
- OCD impedance adjustment.
- Gold contacts
- SDRAMs in 60-ball BGA Package
- RoHs Compliance.

### Description

M2Y1G64TU88G7B and M2Y2G64TU8HG5B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one rank 128Mx64 and two ranks 256Mx64 high-speed memory array. M2Y1G64TU88G7B uses eight 128Mx8 DDR2 SDRAMs and M2Y2G64TU8HG5B uses sixteen 128Mx8 DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 333MHz (or 400MHz/533MHz) clock speeds and achieves high-speed data transfer rates of up to 667Mbps (or 800Mbps/1066Mbps). Prior to any access operation, the device  $\overline{\text{CAS}}$  latency and burst / length /operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1 and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

## Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y1G64TU88G7B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300	128Mx64	GOLD	1.8V	
M2Y1G64TU88G7B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y1G64TU88G7B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				
M2Y2G64TU8HG5B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300	256Mx64			
M2Y2G64TU8HG5B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y2G64TU8HG5B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				

## Pin Description

CK0-CK2 CK0-CK2	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM8	Input Data Mask
$\overline{CAS}$	Column Address Strobe	$\overline{DQS0-DQS8}$	Differential data strobes
$\overline{WE}$	Write Enable	VDD	Power (1.8V)
$\overline{CS0}, \overline{CS1}$	Chip Selects	VREF	Ref. Voltage for SSTL_18 inputs
A0-A9, A0-A13	Address Inputs	VDDSPD	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	VSS	Ground
BA0 ~ BA2	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RESET	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	On-die termination control lines	SA0 ~ SA2	Serial Presence Detect Address Inputs
NC	No Connect		

Note: ODT1, CKE1 and  $\overline{CS1}$  are only support in 2GB module type.

## Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V <sub>REF</sub>	42	NC	82	V <sub>SS</sub>	121	V <sub>SS</sub>	162	NC	202	DM4
2	V <sub>SS</sub>	43	NC	83	DQS4	122	DQ4	163	V <sub>SS</sub>	203	NC
3	DQ0	44	V <sub>SS</sub>	84	DQS4	123	DQ5	164	NC	204	V <sub>SS</sub>
4	DQ1	45	NC	85	V <sub>SS</sub>	124	V <sub>SS</sub>	165	NC	205	DQ38
5	V <sub>SS</sub>	46	NC	86	DQ34	125	DM0	166	V <sub>SS</sub>	206	DQ39
6	DQS0	47	V <sub>SS</sub>	87	DQ35	126	NC	167	NC	207	V <sub>SS</sub>
7	DQS0	48	NC	88	V <sub>SS</sub>	127	V <sub>SS</sub>	168	NC	208	DQ44
8	V <sub>SS</sub>	49	NC	89	DQ40	128	DQ6	169	V <sub>SS</sub>	209	DQ45
9	DQ2	50	V <sub>SS</sub>	90	DQ41	129	DQ7	170	V <sub>DDQ</sub>	210	V <sub>SS</sub>
10	DQ3	51	V <sub>DDQ</sub>	91	V <sub>SS</sub>	130	V <sub>SS</sub>	171	NC,CKE1	211	DM5
11	V <sub>SS</sub>	52	CKE0	92	DQS5	131	DQ12	172	V <sub>DD</sub>	212	NC
12	DQ8	53	V <sub>DD</sub>	93	DQS5	132	DQ13	173	NC	213	V <sub>SS</sub>
13	DQ9	54	BA2	94	V <sub>SS</sub>	133	V <sub>SS</sub>	174	NC	214	DQ46
14	V <sub>SS</sub>	55	NC	95	DQ42	134	DM1	175	V <sub>DDQ</sub>	215	DQ47
15	DQS1	56	V <sub>DDQ</sub>	96	DQ43	135	NC	176	A12	216	V <sub>SS</sub>
16	DQS1	57	A11	97	V <sub>SS</sub>	136	V <sub>SS</sub>	177	A9	217	DQ52
17	V <sub>SS</sub>	58	A7	98	DQ48	137	CK1	178	V <sub>DD</sub>	218	DQ53
18	NC	59	V <sub>DD</sub>	99	DQ49	138	CK1	179	A8	219	V <sub>SS</sub>
19	NC	60	A5	100	V <sub>SS</sub>	139	V <sub>SS</sub>	180	A6	220	CK2
20	V <sub>SS</sub>	61	A4	101	SA2	140	DQ14	181	V <sub>DDQ</sub>	221	CK2
21	DQ10	62	V <sub>DDQ</sub>	102	NC	141	DQ15	182	A3	222	V <sub>SS</sub>
22	DQ11	63	A2	103	V <sub>SS</sub>	142	V <sub>SS</sub>	183	A1	223	DM6
23	V <sub>SS</sub>	64	V <sub>DD</sub>	104	DQS6	143	DQ20	184	V <sub>DD</sub>	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V <sub>SS</sub>
25	DQ17	65	V <sub>SS</sub>	106	V <sub>SS</sub>	145	V <sub>SS</sub>	185	CK0	226	DQ54
26	V <sub>SS</sub>	66	V <sub>SS</sub>	107	DQ50	146	DM2	186	CK0	227	DQ55
27	DQS2	67	V <sub>DD</sub>	108	DQ51	147	NC	187	V <sub>DD</sub>	228	V <sub>SS</sub>
28	DQS2	68	NC	109	V <sub>SS</sub>	148	V <sub>SS</sub>	188	A0	229	DQ60
29	V <sub>SS</sub>	69	V <sub>DD</sub>	110	DQ56	149	DQ22	189	V <sub>DD</sub>	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V <sub>SS</sub>
31	DQ19	71	BA0	112	V <sub>SS</sub>	151	V <sub>SS</sub>	191	V <sub>DDQ</sub>	232	DM7
32	V <sub>SS</sub>	72	V <sub>DDQ</sub>	113	DQS7	152	DQ28	192	RAS	233	NC
33	DQ24	73	WE	114	DQS7	153	DQ29	193	CS0	234	V <sub>SS</sub>
34	DQ25	74	CAS	115	V <sub>SS</sub>	154	V <sub>SS</sub>	194	V <sub>DDQ</sub>	235	DQ62
35	V <sub>SS</sub>	75	V <sub>DDQ</sub>	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	DQS3	76	NC, CS1	117	DQ59	156	NC	196	A13	237	V <sub>SS</sub>
37	DQS3	77	NC,ODT1	118	V <sub>SS</sub>	157	V <sub>SS</sub>	197	V <sub>DD</sub>	238	V <sub>DDSPD</sub>
38	V <sub>SS</sub>	78	V <sub>DDQ</sub>	119	SDA	158	DQ30	198	V <sub>SS</sub>	239	SA0
39	DQ26	79	V <sub>SS</sub>	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V <sub>SS</sub>	200	DQ37		
41	V <sub>SS</sub>	81	DQ33			161	NC	201	V <sub>SS</sub>		

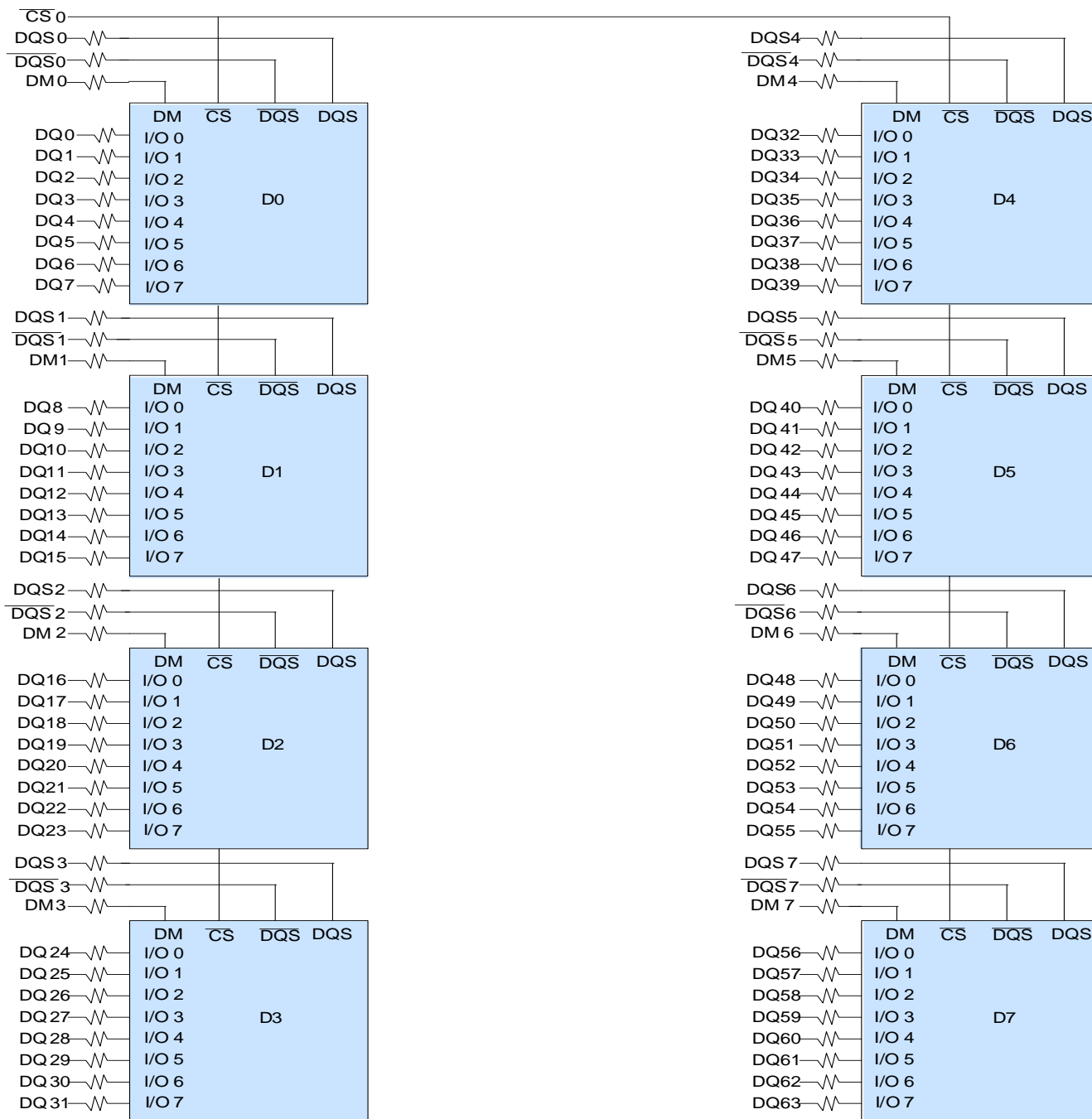
Note:

1. NC = No Connect.
2. CS1, ODT1 and CKE1 (Pins 76, 77 and 171) are only support in 2GB module type.

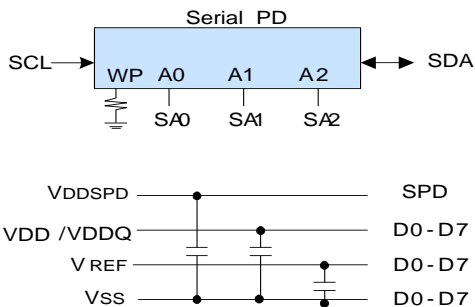
## Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$ , $\overline{CK1}$ , $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. CKE1 apply on 2GB UDIMM only.
$\overline{CS0}$ , $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. $\overline{CS1}$ apply on 2GB UDIMM only.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-18 inputs
VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals. ODT1 apply on 2GB UDIMM only.
BA0 – BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke "Autoprecharge" operation at the end of the Burst Read or Write cycle. If AP is high, Autoprecharge's selected and BA0/BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input /Output pins.
VDD, VSS	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pull-up.
VDDSPD	Supply		Serial EEPROM positive power supply.

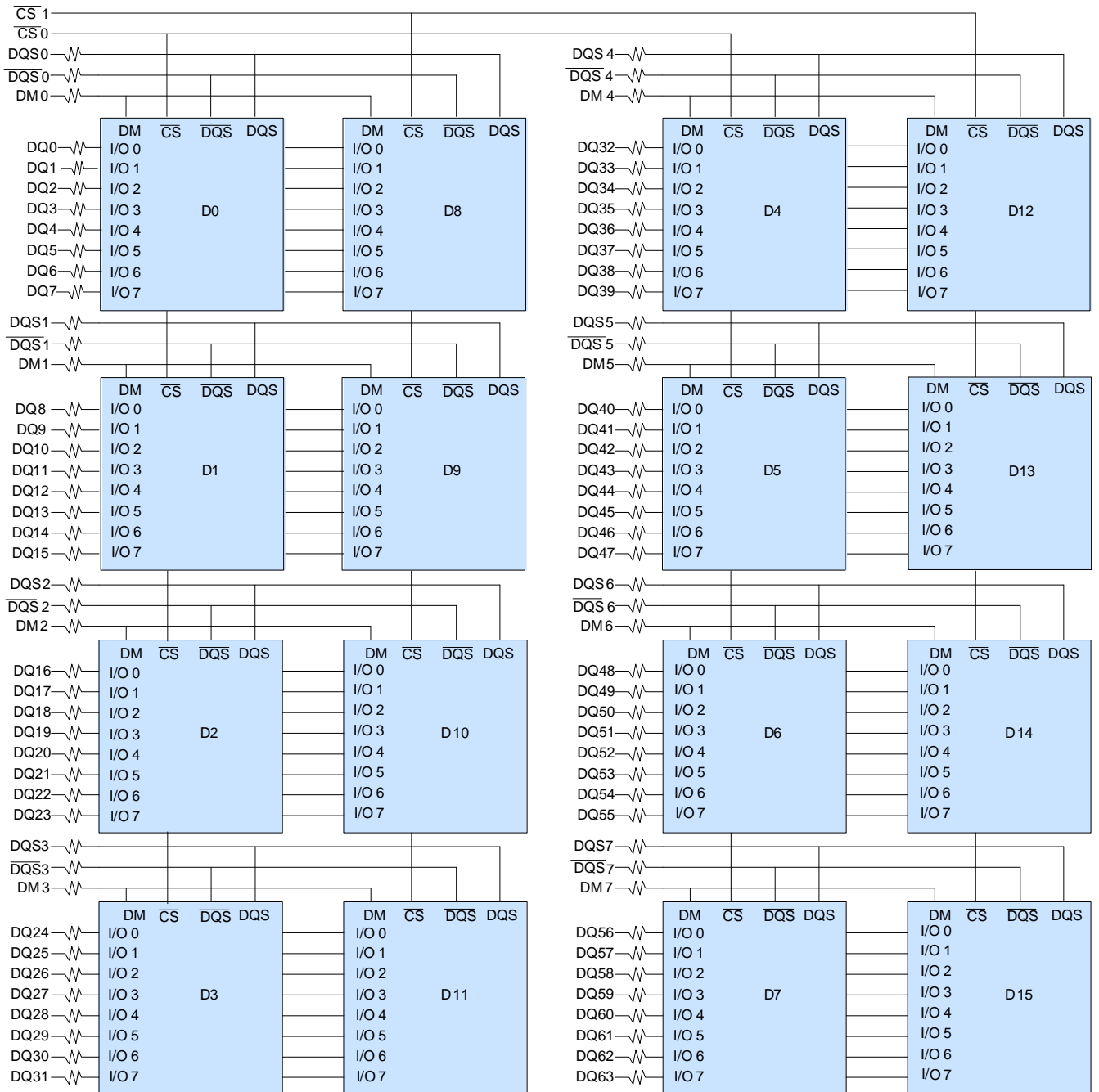
Functional Block Diagram (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)



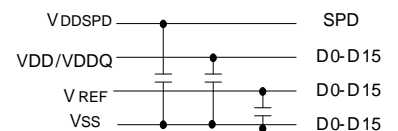
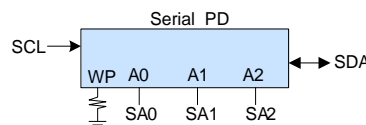
- BA0-BA2 → BA0-BA2: SDRAMs D0-D7
- A0-A13 → A0-A13: SDRAMs D0-D7
- RAS → RAS: SDRAMs D0-D7
- CAS → CAS: SDRAMs D0-D7
- WE → WE: SDRAMs D0-D7
- CKE0 → CKE: SDRAMs D0-D7
- ODT0 → ODT: SDRAMs D0-D7



Functional Block Diagram (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)



- BA0-BA2 → BA0-BA2 : SDRAMs D0-D15
- A0-A13 → A0-A13 : SDRAMs D0-D15
- RAS → RAS : SDRAMs D0-D15
- CAS → CAS : SDRAMs D0-D15
- WE → WE : SDRAMs D0-D15
- CKE0 → CKE : SDRAMs D0-D7
- CKE1 → CKE : SDRAMs D8-D15
- ODT0 → ODT : SDRAMs D0-D7
- ODT1 → ODT : SDRAMs D8-D15



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.5 to 2.3	V
V <sub>DDQ</sub>	Voltage on V <sub>DDQ</sub> supply relative to V <sub>SS</sub>	-0.5 to 2.3	V
V <sub>DDQL</sub>	Voltage on V <sub>DDQL</sub> supply relative to V <sub>SS</sub>	-0.5 to 2.3	V
V <sub>DD</sub>	Voltage on VDD supply relative to V <sub>SS</sub>	-1.0 to +2.3	V

**Note:** Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Operating Conditions

Symbol	Parameter	Rating	Units	Note
T <sub>CASE</sub>	Operating Temperature (Ambient)	0 to 95	°C	1,2,3
T <sub>STG</sub>	Storage Temperature (Plastic)	-55 to 100	°C	
I <sub>L</sub>	Short Circuit Output Current	-5 to 5	Ma	

**Note:**

- Case temperature is measured at top and center side of any DRAMs.
- t<sub>CASE</sub> > 85°C → t<sub>REFI</sub> = 3.9 μs
- All DRAM specification only support 0°C < t<sub>CASE</sub> < 85°C

## DC Electrical Characteristics and Operating Conditions

(T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V <sub>DD</sub>	Supply Voltage	1.7	1.9	V	1
V <sub>DDQ</sub>	Supply Voltage for Output	1.7	1.9	V	1, 3
V <sub>DDL</sub>	Supply Voltage for V <sub>DDQL</sub>	1.7	1.9	V	3
V <sub>REF</sub>	Input Reference Voltage	0.49V <sub>DDQ</sub>	0.51V <sub>DDQ</sub>	Mv	2
V <sub>TT</sub>	Termination Voltage	V <sub>REF</sub> – 0.04	V <sub>REF</sub> + 0.04	V	4
V <sub>IH</sub> (DC)	Input High (Logic1) Voltage	V <sub>REF</sub> + 0.125	V <sub>DDQ</sub> + 0.3	V	
V <sub>IL</sub> (DC)	Input Low (Logic0) Voltage	-0.3	V <sub>REF</sub> – 0.125	V	

**Note:**

- Inputs are not recognized as valid until V<sub>REF</sub> stabilizes.
- V<sub>REF</sub> is expected to be equal to 0.5 V<sub>DDQ</sub> of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V<sub>REF</sub> may not exceed 2% of the DC value.
- V<sub>DDQ</sub> tracks with V<sub>DD</sub>, V<sub>DDL</sub> tracks with V<sub>DD</sub>.
- V<sub>TT</sub> of transmitting device track V<sub>REF</sub> of receiving device.

## Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T <sub>OPR</sub>	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H <sub>OPR</sub>	Operating Humidity (relative)	10 to 90	%	
T <sub>STG</sub>	Storage Temperature (Plastic)	-55 to 100	°C	1
H <sub>STG</sub>	Storage Humidity (without condensation)	5 to 95	%	1
P <sub>BAR</sub>	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

**Note:**

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Up to 9850 ft.
- The component maximum case temperature shall not exceed the value specified in the component spec.

## Operating, Standby, and Refresh Currents

T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = V<sub>DD</sub> = 1.8V ± 0.1V (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300	PC2-6400	PC2-8500	Unit
I <sub>DD0</sub>	Operating Current: one bank; active/precharge; T <sub>rc</sub> = T <sub>rc</sub> (MIN); T <sub>ck</sub> = T <sub>ck</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD1</sub>	Operating Current: one bank; active/read/precharge; Burst = 2; T <sub>rc</sub> = T <sub>rc</sub> (MIN); CL=2.5; T <sub>ck</sub> = T <sub>ck</sub> (MIN); I <sub>OUT</sub> = 0Ma; address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD2P</sub>	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V <sub>IL</sub> (MAX); T <sub>ck</sub> = T <sub>ck</sub> (MIN)	TBD	TBD	TBD	mA
I <sub>DD2N</sub>	Idle Standby Current: CS ≥ V <sub>IH</sub> (MIN); all banks idle; CKE ≥ V <sub>IH</sub> (MIN); T <sub>ck</sub> = T <sub>ck</sub> (MIN); address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD2Q</sub>	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t <sub>ck</sub> = t <sub>ck</sub> (MIN); Other control and address inputs are stable, Data bus inputs are floating.	TBD	TBD	TBD	mA
I <sub>DD3PF</sub>	Active Power-Down Current: All banks open; T <sub>ck</sub> = T <sub>ck</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>low</b> (Fast Power-down Exit).	TBD	TBD	TBD	mA
I <sub>DD3PS</sub>	Active Power-Down Current: All banks open; T <sub>ck</sub> = T <sub>ck</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>high</b> (Slow Power-down Exit).	TBD	TBD	TBD	mA
I <sub>DD3N</sub>	Active Standby Current: one bank; active/precharge; CS ≥ V <sub>IH</sub> (MIN); CKE ≥ V <sub>IH</sub> (MIN); T <sub>rc</sub> = T <sub>ras</sub> (MAX); T <sub>ck</sub> = T <sub>ck</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD4W</sub>	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; T <sub>ck</sub> = T <sub>ck</sub> (MIN)	TBD	TBD	TBD	mA
I <sub>DD4R</sub>	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; T <sub>ck</sub> = T <sub>ck</sub> (MIN); I <sub>OUT</sub> = 0Ma	TBD	TBD	TBD	mA
I <sub>DD5</sub>	Auto-Refresh Current: T <sub>rc</sub> = T <sub>rfc</sub> (MIN)	TBD	TBD	TBD	mA
I <sub>DD6</sub>	Self-Refresh Current: CKE ≤ 0.2V	TBD	TBD	TBD	mA
I <sub>DD7</sub>	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; T <sub>rc</sub> = T <sub>rc</sub> (min); I <sub>OUT</sub> = 0Ma.	TBD	TBD	TBD	mA
<b>Note:</b> Module IDD was calculated from component IDD. It may differ from the actual measurement.					



## Operating, Standby, and Refresh Currents

T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = V<sub>DD</sub> = 1.8V ± 0.1V (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300	PC2-6400	PC2-8500	Unit
I <sub>DD0</sub>	Operating Current: one bank; active/precharge; T <sub>rc</sub> = T <sub>rc</sub> (MIN); T <sub>ck</sub> = T <sub>ck</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD1</sub>	Operating Current: one bank; active/read/precharge; Burst = 2; T <sub>rc</sub> = T <sub>rc</sub> (MIN); CL=2.5; T <sub>ck</sub> = T <sub>ck</sub> (MIN); I <sub>OUT</sub> = 0Ma; address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD2P</sub>	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V <sub>IL</sub> (MAX); T <sub>ck</sub> = T <sub>ck</sub> (MIN)	TBD	TBD	TBD	mA
I <sub>DD2N</sub>	Idle Standby Current: CS ≥ V <sub>IH</sub> (MIN); all banks idle; CKE ≥ V <sub>IH</sub> (MIN); T <sub>ck</sub> = T <sub>ck</sub> (MIN); address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD2Q</sub>	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Other control and address inputs are stable, Data bus inputs are floating.	TBD	TBD	TBD	mA
I <sub>DD3PF</sub>	Active Power-Down Current: All banks open; T <sub>ck</sub> = T <sub>ck</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>low</b> (Fast Power-down Exit).	TBD	TBD	TBD	mA
I <sub>DD3PS</sub>	Active Power-Down Current: All banks open; T <sub>ck</sub> = T <sub>ck</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>high</b> (Slow Power-down Exit).	TBD	TBD	TBD	mA
I <sub>DD3N</sub>	Active Standby Current: one bank; active/precharge; CS ≥ V <sub>IH</sub> (MIN); CKE ≥ V <sub>IH</sub> (MIN); T <sub>rc</sub> = T <sub>ras</sub> (MAX); T <sub>ck</sub> = T <sub>ck</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	TBD	mA
I <sub>DD4W</sub>	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; T <sub>ck</sub> = T <sub>ck</sub> (MIN)	TBD	TBD	TBD	mA
I <sub>DD4R</sub>	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; T <sub>ck</sub> = T <sub>ck</sub> (MIN); I <sub>OUT</sub> = 0Ma	TBD	TBD	TBD	mA
I <sub>DD5</sub>	Auto-Refresh Current: T <sub>rc</sub> = T <sub>rfc</sub> (MIN)	TBD	TBD	TBD	mA
I <sub>DD6</sub>	Self-Refresh Current: CKE ≤ 0.2V	TBD	TBD	TBD	mA
I <sub>DD7</sub>	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; T <sub>rc</sub> = T <sub>rc</sub> (min); I <sub>OUT</sub> = 0Ma.	TBD	TBD	TBD	mA
<b>Note:</b> Module IDD was calculated from component IDD. It may differ from the actual measurement.					

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-5300		PC2-6400		PC2-8500		Unit
		Min.	Max.	Min.	Max.	Min	Max	
T <sub>ck</sub>	Clock Cycle Time (Average)	3000	8000	2500	8000	1875	8000	ps
T <sub>ch</sub>	CK high-level width (Average)	0.48	0.52	0.48	0.52	0.48	0.52	T <sub>ck</sub>
T <sub>cl</sub>	CK low-level width (Average)	0.48	0.52	0.48	0.52	0.48	0.52	T <sub>ck</sub>
WL	Write command to DQS associated clock edge	RL-1		RL-1		RL-1		Nck
T <sub>dqss</sub>	Write command to 1 <sup>st</sup> DQS latching transition	-0.25	0.25	-0.25	0.25	-0.25	0.25	T <sub>ck</sub>
T <sub>dss</sub>	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	T <sub>ck</sub>
T <sub>dsh</sub>	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	T <sub>ck</sub>
T <sub>dqsl,(H)</sub>	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	T <sub>ck</sub>
T <sub>wpre</sub>	Write preamble	0.35	-	0.35	-	0.35	-	T <sub>ck</sub>
T <sub>wpst</sub>	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	T <sub>ck</sub>
T <sub>is</sub>	Address and control input setup time	200	-	175	-	125	-	ps
T <sub>ih</sub>	Address and control input hold time	275	-	250	-	200	-	ps
T <sub>ipw</sub>	Input pulse width	0.6	-	0.6	-	0.6	-	T <sub>ck</sub>
T <sub>ds</sub>	DQ and DM input setup time (differential data strobe)	100	-	50	-	0	-	ps
T <sub>dh</sub>	DQ and DM input hold time(differential data strobe)	175	-	125	-	75	-	ps
T <sub>dipw</sub>	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	T <sub>ck</sub>
T <sub>ac</sub>	DQ output access time from CK/ $\overline{\text{CK}}$	-450	450	-400	400	-350	350	ps
T <sub>dqsck</sub>	DQS output access time from CK/ $\overline{\text{CK}}$	-400	400	-350	350	-350	350	ps
T <sub>hz</sub>	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-	t <sub>AC max</sub>	-	t <sub>ACmax</sub>	-	t <sub>AC max</sub>	ps
T <sub>lz(DQS)</sub>	DQS low-impedance time from CK/ $\overline{\text{CK}}$	t <sub>AC min</sub>	t <sub>AC max</sub>	t <sub>ACmin</sub>	t <sub>ACmax</sub>	t <sub>AC min</sub>	t <sub>AC max</sub>	ps
T <sub>lz(DQ)</sub>	DQ low-impedance time from CK/ $\overline{\text{CK}}$	2t <sub>AC min</sub>	t <sub>AC max</sub>	2t <sub>AC min</sub>	t <sub>AC max</sub>	2t <sub>AC min</sub>	t <sub>AC max</sub>	ps
T <sub>dqsq</sub>	DQS-DQ skew (DQS & associated DQ signals)	-	240	-	200	-	175	ps
T <sub>hp</sub>	Minimum half clk period for any given cycle; defined by clk high (T <sub>ch</sub> ) or clk low (T <sub>cl</sub> ) time	Min(T <sub>ch(abs)</sub> , T <sub>cl(abs)</sub> )	-	Min(T <sub>ch(abs)</sub> , T <sub>cl(abs)</sub> )	-	Min(t <sub>CH(a bs)</sub> , t <sub>CL(a bs)</sub> )	-	ps
T <sub>qhs</sub>	Data hold Skew Factor	-	340	-	300	-	250	ps
T <sub>qh</sub>	Data output hold time from DQS	t <sub>HP</sub> – t <sub>QHS</sub>	-	T <sub>hp</sub> – T <sub>qhs</sub>	-	t <sub>HP</sub> - t <sub>QHS</sub>	-	ps
T <sub>rpre</sub>	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	T <sub>ck</sub>
T <sub>rpst</sub>	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	T <sub>ck</sub>
T <sub>rrd</sub>	Active bank A to Active bank B command	7.5	-	7.5	-	7.5	-	ns
T <sub>faw</sub>	Four Activate Window for 1KB page size products	37.5	-	35	-	35	-	ns
T <sub>ccd</sub>	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$	2	-	2	-	2	-	Nck
T <sub>wr</sub>	Write recovery time without Auto-Precharge	15	-	15	-	15	-	ns
T <sub>dal</sub>	Auto precharge write recovery + precharge time	WR+t <sub>nRP</sub>	-	WR+t <sub>nRP</sub>	-	WR + t <sub>nRP</sub>	-	Nck
T <sub>wtr</sub>	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns
T <sub>trp</sub>	Internal read to precharge command delay	7.5	-	7.5	-	7.5	-	ns
T <sub>cke</sub>	CKE minimum pulse width	3	-	3	-	3	-	Nck
T <sub>xsnr</sub>	Exit self refresh to a Non-read command	T <sub>rfc</sub> +10	-	T <sub>rfc</sub> +10	-	t <sub>RFC</sub> +10	-	ns
T <sub>xsrd</sub>	Exit self refresh to a Read command	200	-	200	-	200	-	Nck
T <sub>xp</sub>	Exit precharge power down to any Non- read command	2	-	2	-	3	-	Nck

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

( $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$ ;  $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ , See AC Characteristics) (Part 2 of 2)

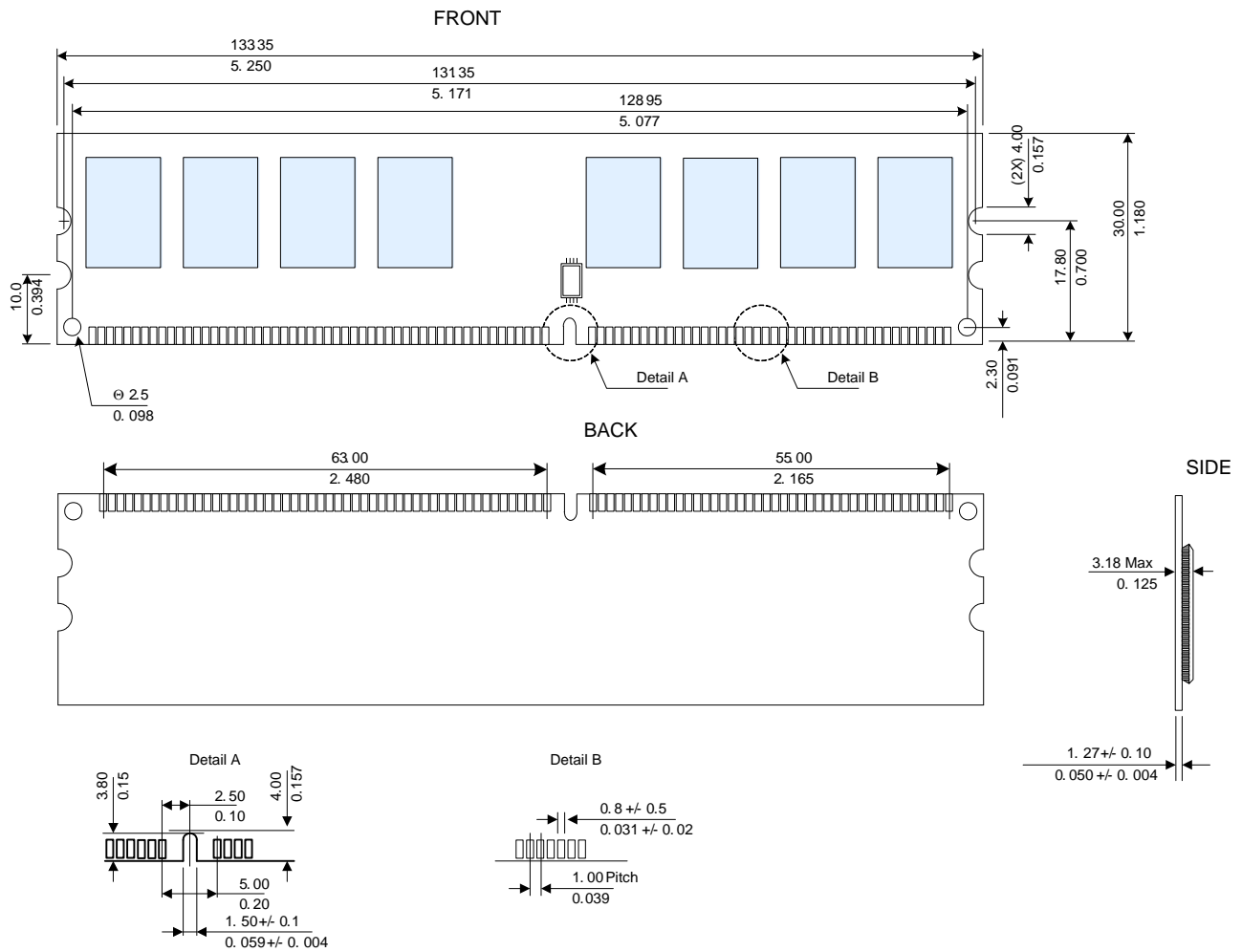
Symbol	Parameter	PC2-5300		PC2-6400		PC2-8500		Unit
		Min.	Max.	Min.	Max.	Min	Max	
$T_{xard}$	Exit active power down to read command	2	-	2	-	3	-	Nck
$T_{xards}$	Exit active power down to read command	7-AL		8-AL		10 - AL	-	Nck
$T_{aond}$	ODT turn-on delay	2	2	2	2	2	2	Nck
$T_{aon}$	ODT turn-on	$T_{ac}(\text{min})$	$T_{ac}(\text{max})+0.7$	$T_{ac}(\text{min})$	$T_{ac}(\text{max})+0.7$	tAC min	tAC max + 2.575	ns
$T_{aonpd}$	ODT turn-on (Power down mode)	$T_{ac}(\text{min})+2$	$2T_{ck} + T_{ac}(\text{max})+1$	$T_{ac}(\text{min})+2$	$2T_{ck} + T_{ac}(\text{max})+1$	tAC min + 2	$3t_{CK} + t_{AC} \text{ max} + 1$	ns
$T_{aofd}$	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	Nck
$T_{aof}$	ODT turn-off	$T_{ac}(\text{min})$	$T_{ac}(\text{max})+0.6$	$T_{ac}(\text{min})$	$T_{ac}(\text{max})+0.6$	tAC min	tAC max + 0.6	ns
$T_{aofpd}$	ODT turn-off (Power down mode)	$T_{ac}(\text{min})+2$	$2.5T_{ck} + T_{ac}(\text{max})+1$	$T_{ac}(\text{min})+2$	$2.5T_{ck} + T_{ac}(\text{max})+1$	tAC min + 2	$2.5t_{CK}+t_{AC} \text{ max} + 1$	ns
$T_{anpd}$	ODT to power down entry latency	3	-	3	-	4	-	Nck
$T_{axpd}$	ODT power down exit latency	8		8		11	-	Nck
$T_{mrd}$	Mode register set command cycle time	2	-	2	-	2	-	Nck
$T_{mod}$	MRS command to ODT update delay	0	12	0	12	0	12	ns
$T_{oit}$	OCD drive mode output delay	0	12	0	12	0	12	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	$T_{is} + T_{ck} + T_{ih}$	-	$T_{is} + T_{ck} + T_{ih}$	-	tis + tCK + tIH	-	ns
$T_{rfc}$	Refresh to active/Refresh command time	127.5		127.5		105		ns
$T_{refi}$	Average Periodic Refresh Interval ( $85^{\circ}\text{C} < T_{CASE} \leq 95^{\circ}\text{C}$ )	3.9		3.9		3.9		$\mu\text{s}$
	Average Periodic Refresh Interval ( $0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$ )	7.8		7.8		7.8		$\mu\text{s}$

## Speed Grade Definition

Symbol	Parameter	PC2-5300		PC2-6400		PC2-8500		Unit
		Min	Max	Min	Max	Min	Max	
$T_{ras}$	Row Active Time	45	70,000	45	70,000	45	70000	ns
$T_{rc}$	Row Cycle Time	60	-	57.5	-	56.25	-	ns
$T_{rzd}$	RAS to CAS delay	15	-	12.5	-	11.25	-	ns
$T_{rp}$	Row Precharge Time	15	-	12.5	-	11.25	-	ns

## Package Dimensions

(Raw Card Version: D, 1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

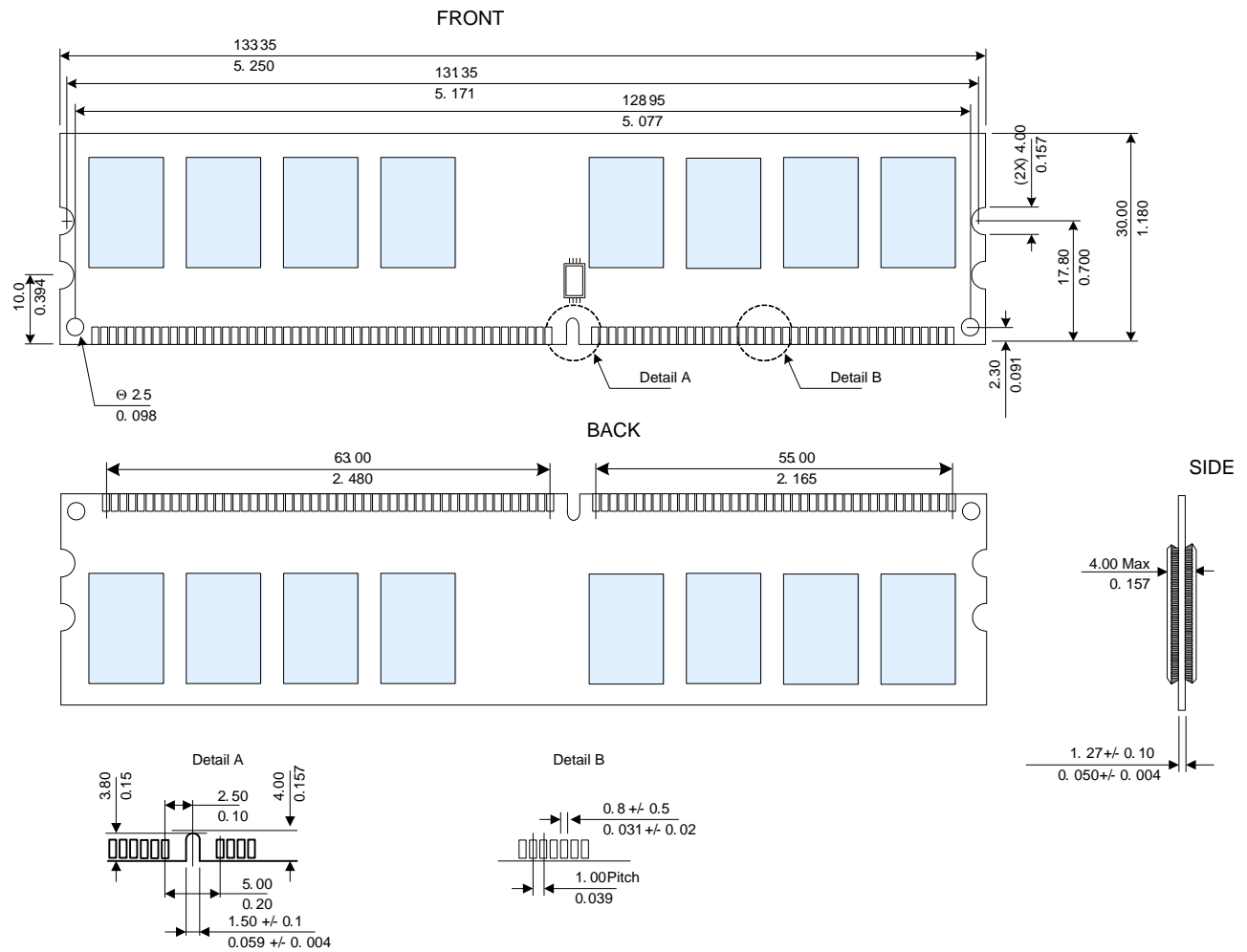


Note: All dimensions are typical with tolerances of  $\pm 0.15$  (0.006) unless otherwise stated

Units: Millimeters (Inches)

## Package Dimensions

(Raw Card Version: E, 2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of  $\pm 0.15$  (0.006) unless otherwise stated

Units: Millimeters (Inches)

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## Revision Log

Rev	Date	Modification
0.1	01/2010	Preliminary Edition